Amendments to the Abstract:

Please replace the Abstract with the following amended Abstract as follows:

A cache memory system and method includes a DRAM having a plurality of banks, ~~each of which may be refreshed under control of a refresh controller. In addition to the usual components of a DRAM, The cache memory system~~and it also includes 2 SRAMs each having a capacity that is equal to the capacity of each bank of the DRAM. In operation, data read from a bank of the DRAM are stored in one of the SRAMs so that repeated hits to that bank are cached by reading from the SRAM. In the event of a write to a bank that is being refreshed, the write data are stored in one of the SRAMs. After the refresh of the bank has been completed, the data stored in the SRAM are transferred to the DRAM bank. A subsequent read or write to a second DRAM bank undergoing refresh and occurring during the transfer of data from an SRAM to the DRAM is stored in either the second bank or the other SRAM. ~~If, however, the second bank is being refreshed, the data are stored in the other SRAM. By the time data have been stored in the SRAM, the SRAM previously used to store write data has transferred the data to the first DRAM bank and in thus available to store a subsequent write. Therefore, an SRAM bank is always available to store write data in the event the DRAM bank to which the data are directed is being refreshed.~~